

Atty. Dkt. No. 035905-0104

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

Applicant: Thomas H. LEE et al.  
Title: DENSE ARRAYS AND CHARGE  
STORAGE DEVICES, AND  
METHODS FOR MAKING SAME  
Appl. No.: 09/927,648  
Filing Date: 08/13/2001  
Examiner: Howard Weiss  
Art Unit: 2818

**INFORMATION DISCLOSURE STATEMENT**  
**UNDER 37 CFR §1.56**

Commissioner for Patents  
PO Box 1450  
Alexandria, Virginia 22313-1450

Sir:

Submitted herewith on Form PTO/SB/08 is a listing of documents known to Applicants in order to comply with Applicants' duty of disclosure pursuant to 37 CFR §1.56. A copy of each listed document is being submitted to comply with the provisions of 37 CFR §1.97 and §1.98.

The submission of any document herewith, which is not a statutory bar, is not intended as an admission that such document constitutes prior art against the claims of the present application or that such document is considered material to patentability as defined in 37 CFR §1.56(b). Applicants do not waive any rights to take any action which would be appropriate to antedate or otherwise remove as a competent reference any document which is determined to be a *prima facie* art reference against the claims of the present application.

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**TIMING OF THE DISCLOSURE**

The listed documents are being submitted in compliance with 37 CFR §1.97(c), before the mailing date of either a final action under 37 CFR §1.113, a notice of allowance under 37 CFR §1.113, or an action that otherwise closes prosecution in the application.

Applicants respectfully request that any listed document be considered by the Examiner and be made of record in the present application and that an initialed copy of Form PTO/SB/08 be returned in accordance with MPEP §609.

**FEE**

A fee in connection with submission of an information disclosure statement under 37 CFR §1.97(c) in the amount of \$180.00 in accordance with 37 CFR §1.17(p) is attached.

The Commissioner is hereby authorized to charge any additional fees which may be required regarding this application under 37 CFR §§ 1.16-1.17, or credit any overpayment, to Deposit Account No. 19-0741. Should no proper payment be enclosed herewith, as by a check being in the wrong amount, unsigned, post-dated, otherwise improper or informal or even entirely missing, the Commissioner is authorized to charge the unpaid amount to Deposit Account No. 19-0741.

Respectfully submitted,

Date 7/15/03

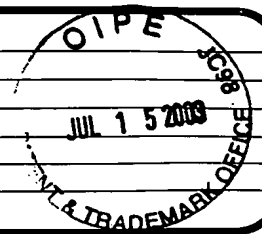
By 

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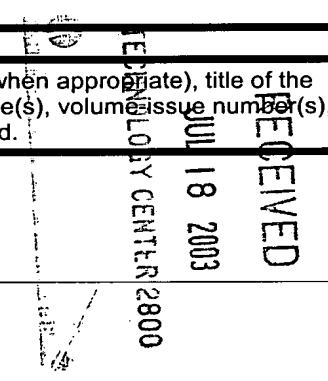
Substitute for form 1449B/PTO <b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b> Date Submitted: 7/15/03 (use as many sheets as necessary)				<b>Complete if Known</b> Application Number: 09/927,648 Filing Date: 08/13/2001 First Named Inventor: Thomas H. Lee Group Art Unit: 2818 Examiner Name: Howard Weiss Attorney Docket Number: 035905-0104	
Sheet	1	of	1		



U.S. PATENT DOCUMENTS						
Examiner Initials*	Cite No. <sup>1</sup>	U.S. Patent Document		Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number	Kind Code <sup>2</sup> (if known)			
	C18	6,323,515	B1	Yamazaki, et al	11/27/01	
	C19	6,577,531	B2	Kato	6/10/03	
	C20	6,509,602	B2	Yamazaki, et al	1/21/03	
	C21	6,472,684	B1	Yamazaki, et al	10/29/02	
	C22	6,498,369	B1	Yamazaki, et al	12/24/02	
	C23	6,255,705	B1	Zhang, et al	7/3/01	

FOREIGN PATENT DOCUMENTS						
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		Office e <sup>3</sup>	Number <sup>4</sup>	Kind Code <sup>5</sup> (if known)		
	C24		EP 1017 100	A1	Shimoda, Tatsuya et al	7/5/00

NON PATENT LITERATURE DOCUMENTS			
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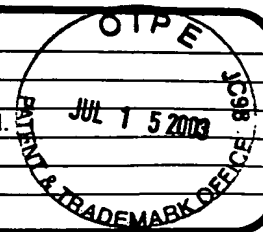
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**INFORMATION DISCLOSURE  
 STATEMENT BY APPLICANT**

Date Submitted: November 27, 2001

(use as many sheets as necessary)

**Complete If Known**

Application Number	09/927,648
Filing Date	08/13/2001
First Named Inventor	Thomas H. Lee et al.
Group Art Unit	2818
Examiner Name	Unassigned
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Sheet 1 of 7

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	A51	5,427,979		Chang	6/27/1995	
	A52	5,070,384		McCollum et al.	12/3/1991	
	A53	4,498,226		Inoue et al.	2/12/1985	
	A54	4,489,478		Sakurai	12/25/1984	
	A55	4,272,880		Pashley	6/16/1981	
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	A79	5,070,383		Sinar et al.	5,070,383	
	A80	5,311,039		Kimura et al.	5,311,039	
	A81	5,334,880		Abadeer et al.	5,334,880	
	A82	5,391,907		Jang	2/21/1995	
	A83	5,441,907		Sung et al.	5,441,907	
	A84	5,463,244		De Araujo et al.	5,463,244	
	A85	5,536,968		Crafts et al.	7/16/1996	
	A86	5,675,547		Koga	10/7/1997	
	A87	5,737,259		Chang	4/7/1998	
	A88	5,751,012		Wolstenholme et al.	5/12/1998	
	A89	5,776,810		Guterman et al.	7/7/1998	
	A90	5,835,396		Zhang	11/10/1998	

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				Application Number	09/927,648
				Filing Date	08/13/2001
				First Named Inventor	Thomas H. Lee et al.
				Group Art Unit	2818
				Examiner Name	Unassigned
				Attorney Docket Number	035905/0104
Sheet	2	of	7		

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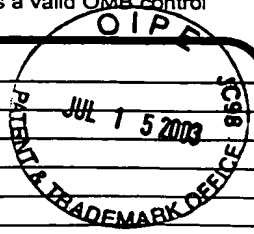
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	A115	JOHN H. DOUGLAS: "The Route to 3-D Chips," High Technology, September 1983, pgs. 55-59, Vol. 3, No. 9, High Technology Publishing Corporation, Boston, MA		
	A116	M. ARIENZO et al.: "Diffusion of Arsenic in Bilayer Polycrystalline Silicon Films," J. Appl. Phys., January 1984, pgs. 365-369, Vol. 55, No. 2, American Institute of Physics		
	A117	O. BELLEZZA et al.: "A New Self-Aligned Field Oxide Cell for Multimegabit Eeproms," IEDM, pgs. 579-582, IEEE		
	A118	S.D. BROTHERTON et al.: "Excimer-Laser-Annealed Poly-Si Thin-Film Transistors," IEEE Transactions on Electron Devices, February 1993, pgs. 407-413, Vol. 40, No. 2, IEEE		
	A119	P. CANDELIER et al.: "Simplified 0.35-μm Flash EEPROM Process Using High-Temperature Oxide (HTO) Deposited by LPCVD as Interpoly Dielectrics and Peripheral Transistors Gate Oxide," IEEE Electron Device Letters, July 1997, pgs. 306-308, Vol. 18, No. 7, IEEE		
	A120	MIN CAO et al.: "A High-Performance Polysilicon Thin-Film Transistor Using XeCl Excimer Laser Crystallization of Pre-Patterned Amorphous Si Films," IEEE Transactions on Electron Devices, April 1996, pgs. 561-567, Vol. 43, No. 4, IEEE		
	A121	MINO CAO et al.: "A Simple EEPROM Cell Using Twin Polysilicon Thin Film Transistors," IEEE Electron Device Letters, August 1994, pgs. 304-306, Vol. 15, No. 8, IEEE		
	A122	BOMY CHEN et al.: "Yield Improvement for a 3.5-ns BICMOS Technology in a 200-mm Manufacturing Line," IBM Technology Products, 1993, pgs.301-305, VLSITSA		
	A123	VICTOR W.C. CHAN et al.: "Three Dimensional CMOS Integrated Circuits on Large Grain Polysilicon Films," IEDM, 2000, IEEE		
	A124	BOAZ EITAN et al.: "Alternate Metal Virtual Ground (AMG) - A New Scaling Concept for Very High-Density EPROM's," IEEE Electron Device Letters, pgs. 450-452, Vol. 12, No. 8, August 1991, IEEE		

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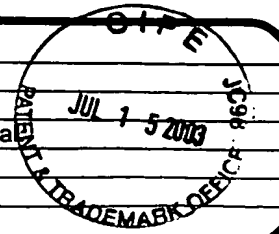
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		Filing Date	08/13/2001
		First Named Inventor	Thomas H. Lee et al.
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		Examiner Name	Unassigned
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		Attorney Docket Number	035905/0104



OTHER PRIOR ART – NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No. <sup>1</sup>	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.) date, page(s), volume-issue number(s), publisher, city and/or country where published.	T <sup>2</sup>
	A125	BOAZ EITAN et al.: "Multilevel Flash cells and their Trade-offs," IEEE Electron Device Letters , pgs. 169-172, 1996, IEEE	
	A126	DR. HEINRICH ENDERT: "Excimer Lasers as Tools for Material Processing in Manufacturing," Technical Digest: International Electron Devices Meeting, 1985, pgs. 28-29, Washington, DC, December 1-4, 1985, Göttingen, Germany	
	A127	DOV FROHMAN-BENTCHKOWSKY: "A Fully Decoded 2048-Bit Electrically Programmable FAMOS Read-Only Memory," IEEE Journal of Solid-State Circuits, pgs. 301-306, Vol. sc-6, No. 5, October 1971	
	A128	G.K. GIUST et al.: "Laser-Processed Thin-Film Transistors Fabricated from Sputtered Amorphous-Silicon Films," IEEE Transactions on Electron Devices, pgs. 207-213, Vol. 47, No. 1, January 2000, IEEE	
	A129	G.K. GIUST et al.: "High-Performance Thin-Film Transistors Fabricated Using Excimer Laser Processing and Grain Engineering," IEEE Transactions on Electron Devices, pgs. 925-932, Vol. 45, No. 4, April 1998, IEEE	
	A130	G.K. GIUST et al.: "High-Performance Laser-Processed Polysilicon Thin-Film Transistors," IEEE Electron Device Letters, pgs. 77-79, Vol. 20, No. 2, February 1999, IEEE	
	A131	FUMIHIKO HAYASHI et al.: "A Self-Aligned Split-Gate Flash EEPROM Cell with 3-D Pillar Structure," 1999 Symposium on VLSI Technology Digest of Technical Papers, pgs. 87-88, Stanford University, Stanford, CA 94305, USA	
	A132	STEPHEN C.H. HO et al.: "Thermal Stability of Nickel Silicides in Different Silicon Substrates," Department of Electrical and Electronic Engineering, pgs. 105-108, 1998, IEEE	
	A133	J. ESQUIVEL et al. "High Density Contactless, Self Aligned EPROM Cell Array Technology," Texas Instruments (Dallas), IEDM 86, pgs. 592-595, 1986, IEEE	

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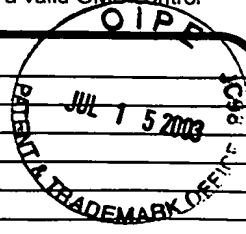
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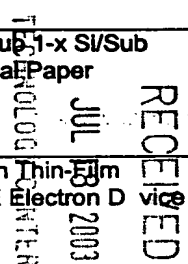
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	A134	R. KAZEROUNIAN et al.: Alternate Metal Virtual Ground EPROM Array Implemented in a 0.8µm Process for Very High Density Applications," IEDM 91, pgs. 311-314, 1991, IEEE	
	A135	CHANG-DONG KIM et al.: "Short-Channel Amorphous-Silicon Thin-Film Transistors," IEEE Transactions on Electron Devices, pgs. 2172-2176, Vol. 43, No. 12, December 1996, IEEE	
	A136	JOHAN H. KLOOTWIJK et al.: "Deposited Inter-Polysilicon Dielectrics for Nonvolatile Memories," IEEE Transactions on Electron Devices, pgs. 1435-1445, Vol. 46, No. 7, July 1999, IEEE	
	A137	WEBPAGE - JA-HUM KU et al.: "High Performance pMOSFETs With Ni(Si/sub x/Ge/sub 1-x Si/Sub 0.8/Ge/sub 0.2/ gate, IEEE Xplore Citation," VLSI Technology, 200. Digest of Technical Paper Symposium on page(s): 114-115 June 13-15 2000	
	A138	NAE-IN LEE et al.: "High-Performance EEPROM's Using N- and P-Channel Polysilicon Thin-Film Transistors with Electron Cyclotron Resonance N2O-Plasma Oxide," pgs. 15-17, IEEE Electron Device Letters, Vol. 20, No. 1, January 1999, IEEE	
	A139	JIN-WOO LEE et al.: "Improved Stability of Polysilicon Thin-Film Transistors under Self-Heating and High Endurance EEPROM Cells for Systems-On-Panel," IEEE Electron Device Letters, 1998, pgs. 265-268, IEEE	
	A140	SEOK-WOON LEE et al.: "Pd induced lateral crystallization of Amorphous Si Thin Films," Appl. Phys. Lett. 66 (13), pgs. 1671-1673, 27 March 1995, American Institute of Physics	
	A141	K. MIYASHITA et al.: "Optimized Halo Structure for 80 nm Physical Gate CMOS Technology with Indium and Antimony Highly Angled Ion Implantation," IEDM 99-645, pgs. 27.2.1-27.2.4, 1999, IEEE	
	A142	N.D. YOUNG et al.: "The Fabrication and Characterization of EEPROM Arrays on Glass Using a Low-Temperature Poly-Si TFT Process," IEEE Transactions on Electron Devices, pgs. 1930-1936, Vol. 43, No. 11, November 1996, IEEE	



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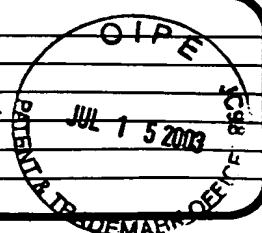
<sup>1</sup> Unique citation designation number. <sup>2</sup> See attached Kinds of U.S. Patent Documents. <sup>3</sup> Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). <sup>4</sup> For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document.

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<b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b>  Date Submitted: <u>November 27, 2001</u>  (use as many sheets as necessary)				Application Number	09/927,648
				Filing Date	08/13/2001
				First Named Inventor	Thomas H. Lee et al.
				Group Art Unit	2818
				Examiner Name	Unassigned
Sheet	6	of	7	Attorney Docket Number	035905/0104



## OTHER PRIOR ART - NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No. <sup>1</sup>	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.) date, page(s), volume-issue number(s), publisher, city and/or country where published.	T <sup>2</sup>
	A143	JUNG-HOON OH et al.: "A High-Endurance Low-Temperature Polysilicon Thin-Film Transistor EEPROM Cell," pgs. 304-306, IEEE Electron Device Letters, Vol. 21, No. 6, June 2000, IEEE	
	A144	WEBPAGE - M.C. POON. et al.: "Thermal Stability of Cobalt and Nickel Silicides in Amorphous Crystalline Silicon," pg. 1, IEEE Xplore, Electron Devices Meeting, 1997, Proceedings, 19 Hong Kong, 2000, IEEE	
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	A147	SEUNGHEON SONG et al.: "High Performance Transistors with State-of-the-Art CMOS Technologies," IEDM 99, pgs. 427-430, 1999, IEEE	
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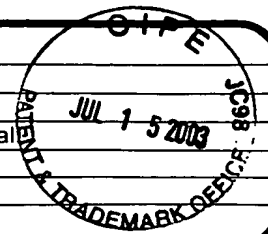
Date Submitted: June 11, 2002

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**Complete if Known**

Application Number 09/927,648  
 Filing Date 08/13/2001  
 First Name and Inventor Thomas H. LEE et al.  
 Group Art Unit 2818  
 Examiner Name Unassigned  
 Attorney Docket Number 035905-0104

Sheet 1 of 7



**U.S. PATENT DOCUMENTS**

Examiner Initials*	Cite No. <sup>1</sup>	U.S. Patent Document		Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number	Kind Code <sup>2</sup> (if known)			
	B1	4,500,905		Shibata		
	B2	6,185,122		Johnson et al.		
	B3	3,414,892		McCormack et al.	12/13/1968	
	B4	3,432,827		Sarno	3/11/1969	
	B5	4,535,424		Reid		
	B6	4,630,096		Drye		
	B7	4,672,577		Hirose		
	B8	4,710,798		Marcantonio		
	B9	4,811,082		Jacobs		
	B10	5,001,539		Inoue et al.		
	B11	5,089,862		Warner, Jr. et al.		
	B12	5,160,987		Pricer et al.		
	B13	5,191,405		Tomita et al.		
	B14	5,202,754		Bertin et al.		
	B15	5,266,912		Kledzik		
	B16	5,283,458		Stokes et al.		
	B17	5,398,200		Mazure et al.		
	B18	5,422,435		Takiar et al.		
	B19	5,426,566		Beilstein, Jr		
	B20	5,434,745		Shokrgozar et al.		
	B21	5,453,952		Okudaira		
	B22	5,455,455		Kurtz et al.		
	B23	5,468,997		Imai et al.		
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	B25	5,481,133		Hsu		
	B26	5,495,398		Takiar et al.		
	B27	5,502,289		Takiar et al.		
	B28	5,523,622		Harada et al.		
	B29	5,523,628		Williams et al.		
	B30	5,552,963		Burns		
	B31	5,561,622		Bertin et al.		
	B32	5,581,498		Ludwig et al.		
	B33	5,585,675		Knopf		
	B34	5,612,570		Eide et al.		
	B35	5,654,220		Leedy		
	B36	5,693,552		Hsu		
	B37	5,696,031		Wark		
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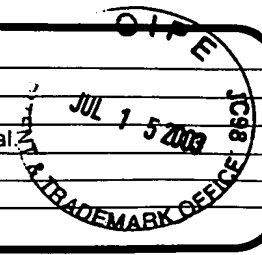
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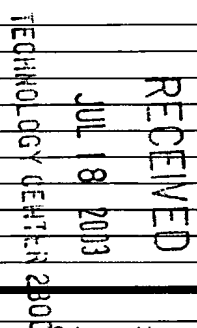
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				Application Number	09/927,648
				Filing Date	08/13/2001
				First Name and Inventor	Thomas H. LEE et al.
				Group Art Unit	2818
				Examiner Name	Unassigned
Sheet	2	of	7	Attorney Docket Number	035905-0104



U.S. PATENT DOCUMENTS					
	U.S. Patent Document				
	B43	5,969,380		Syyedy	
	B44	5,976,953		Zavracky et al.	
	B45	5,985,693		Leedy	
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	B49	6,133,640		Leedy	
	B50	6,351,028		Akram	
	B51	6,281,042	B1	Ahn et al.	
	B52	6,291,858	B1	Ma et al.	
	B53	6,307,257	B1	Huang et al.	
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	B55	6,322,903	B1	Siniaguine et al.	
	B56	6,337,521	B1	Masuda	
	B57	6,353,265	B1	Michii	
	B58	6,355,501	B1	Fung et al.	
	B59	6,197,641	B1	Hergenrother et al.	



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Examiner Initials*	Cite No. <sup>1</sup>	Foreign Patent Document			Name of Patentee or Applicant of Cited Documents	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T <sup>6</sup>
		Office <sup>3</sup>	Number <sup>4</sup>	Kind Code <sup>5</sup> (if known)				
	B60	EPO	0 073 486	A2	Toyama et al.	8-26-1982		
	B61	JP	61-222216		Yohehara	10-2-1986		
	B62	WO	94/26083		Carson et al.	11-10-1994		
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	B69	JP	6-22352		Toshiba			
	B70	EPO	0 387 834	A2	Wada	9-14-1990		

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				First Named Inventor	Thomas H. LEE et al.
				Group Art Unit	2818
				Examiner Name	Unassigned
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Sheet	3	of	7		

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	B71	ABOU-SAMRA S.J.: "3D CMOS SOI for High Performance Computing", Low Power Electronics and Design Proceedings, 1998.	
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				Filing Dat	08/13/2001
				First Nam d Inv nt r	Thomas H. LEE et al.
				Group Art Unit	2818
				Examiner Name	Unassigned
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	B83	CARTER WILLIAM H.: "National Science Foundation (NSF) Forum on Optical Science and Engineering", Proceedings SPIE - The International Society for Optical Engineering, Vol. 2524, July 11 - 12 1995, (Article by N. Joverst titled "Manufacturable Multi-Material Integration Compound Semi-conductor Devices Bonded to Silicon Circuitry".	
	B84	HAYASHI Y.: "A New Three Dimensional IC Fabrication Technology, Stacking Thin Film Dual-CMOS Layers", IEDM, 1991, pgs. 25.6.1 - 25.6.4.	
	B85	REBER M.: "Benefits of Vertically Stacked Integrated Circuits for Sequential Logic", IEEE, 1996, pgs. 121-124.	
	B86	STERN JON M.: "Design and Evaluation of an Epoxy Three-dimensional Multichip Module, IEEE Transactions on Components, Packaging, and Manufacturing Technology - Part B, Vol. 19, No. 1, February 1996, pgs 188-194.	
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Examiner Signature	Date Considered
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				<b>Group Art Unit</b>	2818
(use as many sheets as necessary)				<b>Examiner Name</b>	Unassigned
				<b>Attorney Docket Number</b>	035905-0104
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B100	Abstract SAKAMATO K.: "Architecture of Three Dimensional Devices", Journal: Bulletin of the Electrotechnical Laboratory, Vol. 51, No. 1, 1987, pgs. 16-29.
B101	Abstract "Wide Application of Low-Cost Associative Processing Associative Processing Seen", Electronic Engineering Times, August 26, 1996, pg. 43.
B102	Abstract "Interconnects & Packaging", Electronic Engineering Times, November 27, 1995, pg. 43.
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B104	Abstract "Module Pact Pairs Cubic Memory with VisionTek", Semiconductor Industry & Business Survey, Vol. 17, No. 15, October 23, 1995.
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B106	Abstract "Technologies Will Pursue Higher DRAM Densities", Electronic News (1991), December 4, 1994, pg. 12.

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<b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b>				Application Number	09/927,648
				Filing Date	08/13/2001
				First Named Inventor	Thomas H. LEE et al.
				Group Art Unit	2818
				Examiner Name	Unassigned
Date Submitted: June 11, 2002				Attorney Docket Number	
(use as many sheets as necessary)				035905-0104	
Sheet	6	of	7		

B107	Abstract "Looking Diverse Storage", Electronic Engineering Times, October 31, 1994, pg. 44.
B108	Abstract "Special Report: Memory Market Startups Cubic Memory: 3D Space Savers", Semiconductor Industry & Business Survey, Vol. 16, No. 13, September 12, 1994.
B109	Abstract "Technique Boosts 3D Memory Density", Electronic Engineering Times, August 29, 1994, pg. 16.
B110	Abstract "Memory Packs Poised 3D Use", Electronic Engineering Times, December 7, 1992, pg. 82.
B111	Abstract "MCMs Hit the Road", Electronic Engineering Times, June 15, 1992, pg. 45.
B112	Abstract "IEDM Ponders the 'Gigachip' Era", Electronic Engineering Times, January 20, 1992, pg. 33.
B113	Abstract "Tech Watch: 1-Gbit DRAM in Sight", Electronic World News, December 16, 1991, pg. 20.
B114	Abstract "MCMs Meld into Systems", Electronic Engineering Times, July 22, 1991, pg. 35.
B115	Abstract "Systems EEs See Future in 3D", Electronic Engineering Times, September 24, 1990, pg. 37.
B116	Patent Application, NISHIURA, US 2001/00054759 A1.
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B118	Patent Application, FUJIMOTO et al, US 2002/0027275 A1.

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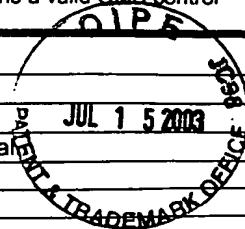
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		Application Number Filing Date First Named Inventor Group Art Unit Examiner Name Attorney Docket Number	09/927,648 08/13/2001 Thomas H. LEE et al. 2818 Unassigned 035905-0104
Sheet	7	of	7



B119	Patent Application, AKRAM, US 2002/0030262 A1.
B120	Patent Application, AKRAM, US 2002/0030263 A1.
B121	Patent Application, LEEDY, US 2001/0033030 A1.
B122	Chan et al. "Three Dimensional CMOS integrated Circuits on Large Grain Polysilicon Films" IEEE, Hong Kong University of Science and Technology 2000 IEEE

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